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PTO/SB/08A (10-96)

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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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|----------------------|------------------|
| Application Number   | 10/045,055       |
| Filing Date          | January 15, 2002 |
| First Named Inventor | Benoudiz         |
| Group Art Unit       | 2133             |
| Examiner Name        |                  |

Attorney Docket Number

24773

Previously V02/16

### U.S. PATENT DOCUMENTS

| Examiners Initials | Cite No. <sup>1</sup> | U.S. Patent Document |                                   | Name of Patentee or Applicant of Cited Document | Date of Publication of Cited Document MM-DD-YYYY | Pages, columns, lines. Where Relevant Passages or Relevant Figures Appear |
|--------------------|-----------------------|----------------------|-----------------------------------|---|--|---|
|                    |                       | Number               | Kind Code <sup>2</sup> (if known) |   |  |   |
| CK                 | AA                    | 4,937,765            |                                   | Shupe et al                                     | 06-26-1990                                       |   |
| CK                 | AB                    | 5,202,889            |                                   | Aharon et al                                    | 04-13-1993                                       |   |
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### OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

|                   |                       |   |                |
|-------------------|-----------------------|---|----------------|
| Examiner Initials | Cite No. <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published. | T <sup>2</sup> |
| CK                | AG                    | Benjamin et al, A Study in Coverage-Driven Test Generation, DAC, 1999, pp. 970 – 975  |                |
| CK                | AH                    | Debany Jr. et al, Design Verification Using Logic Tests, IEEE, 1992, pp. 17 – 24  |                |
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| CK                | AL                    | Sneed, State Coverage of Embedded Realtime Programs, Proc. 2 <sup>nd</sup> Workshop on Software Testing, Verification & Analysis, 1988, pp 245  |                |

Examiner Signature

Chuck Kendall

Date Considered

8/26/04

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